

Q.31 Write a VHDL code for full adder using data flow modeling.

Q.32 Differentiate between CPLD and FPGA?

SECTION-D

Note: Long answer type questions. Attempt any three questions out of four questions. (3x10=30)

Q.33 Explain behavioural, dataflow and structural modeling techniques.

Q.34 Develop a VHDL code for 4:1 Multiplexer using Behavioural modeling.

Q.35 Write a difference between signal and variable.

Q.36 Write a short note on the following. (Any two)

i) Entity

ii) Architecture

iii) Packages

(200)

(4)

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6th Sem.

Subject : VLSI SYSTEM DESIGN

Time : 3 Hrs.

M.M. : 100

SECTION-A

Note: Objective type questions. All questions are compulsory. (10x1=10)

Q.1 Write the difference between ROM and RAM.

Q.2 Counters are for counting a sequence of values. (T/F)

Q.3 What is overloading in VHDL.

Q.4 What is CPLD?

Q.5 How does PLA differ from ROM?

Q.6 Full form of GAL.

Q.7 Write the significance of HDL in digital design.

Q.8 Define the clock.

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Q.9 FPGA stands for_____.

Q.10 Explain the use of WAIT statement with example.

SECTION-B

Note:Very Short answer type questions. Attempt any ten questions out of twelve questions.
(10x2=20)

Q.11 Write the use in VHDL.

Q.12 Define Concurrent Statements.

Q.13 What are various sequential statements?

Q.14 What is operator overloading?

Q.15 What is CPLD?

Q.16 Write the need of Cad tool?

Q.17 What is delay?

Q.18 What is overloading in VHDL.(T/F)

Q.19 What is the Data flow modeling.

Q.20 How does PLA differ from ROM.

Q.21 Explain the inertial delay.

Q.22 PEEL stands for_____.

SECTION-C

Note:Short answer type questions. Attempt any eight questions out of ten questions. (8x5=40)

Q.23 Explain the different type of operations in VHDL.

Q.24 Write a data flow model for 3 to 8 decoder.

Q.25 Explain the internal architecture of FPGA.

Q.26 Write a VHDL program to design 2-bit comparator circuit.

Q.27 Explain various data types in VHDL.

Q.28 Write the behaviour model of 4 to 1 MUX using IF statement.

Q.29 Explain various data types in VHDL.

Q.30 Write the design steps of counters.